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FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation; and ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW (EDL)
(Consolidated with Case No. C 07-2664 JSW)

DECLARATION OF DR. RICHARD A. BLANCHARD IN SUPPORT OF FAIRCHILD'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

Date: June 4, 2008
Time: 2:00 p.m.
Courtroom: Hon. Jeffrey S. White

I, Dr. Richard A. Blanchard, declare as follows:

Biography

1. I have been retained as an expert regarding semiconductor technology by Defendant and Counterclaimant Fairchild Semiconductor Corporation ("Fairchild"). This Declaration is submitted in support of Fairchild's Responsive Claim Construction Brief ("Responsive Brief"). I have personal knowledge of the matters stated herein and if called to testify as a witness, I could and would competently testify thereto.

2. I received a BSEE degree in 1968 and an MSEE degree in 1970 from MIT, and a PhD in Electrical Engineering from Stanford University in 1982. I was an Associate Professor, Assistant Division Chairman of the Engineering & Technology Division at Foothill College from 1974 to 1978, where among other things, I developed the curriculum for the Semiconductor Technology Program.

3. I have over 35 years of experience in the semiconductor and electronics industries. I am an exclusive expert at the Silicon Valley Expert Witness Group, Inc. ("SVEWG") and have extensive consulting experience since 1998 for SVEGW. Prior to working for SVEWG, I was Principal Engineer and Division Manager of the Electrical/Electronic Division of Failure Analysis (Exponent) Associates, Inc., from 1991 to 1998. As Division Manager, my duties included failure analysis and reverse engineering of solid-state electronic components and circuits, failure analysis of electric and electronic systems, subsystems, and components, and consulting with respect to Power MOS and Smart Power Technologies. Prior to that, I was employed by IXYS Corporation from 1987-1991, by Siliconix, Inc., from 1982-1987, by Supertex, Inc., from 1976-1982, by Cognition, Inc., from 1976 to 1978, by Foothill College from 1974-1978, as an independent consultant to the semiconductor industry from 1974-1976 and by Fairchild Semiconductor from 1970-1974.

4. I have testified in court and in deposition on numerous occasions as an expert witness, and I have served as a court-appointed special master. I have published several books and numerous articles on semiconductor design and process development, as well as failure analysis. I hold more than 130 U.S. patents on semiconductor technology. I am a member of the IEEE, the Electrostatic Discharge Society, and the International Microcircuits and Packaging Society, and the Electron Device Failure Analysis Society (EDFAS).

Task

5. I was retained by the law firm of Townsend and Townsend and Crew LLP ("Townsend"), counsel to Fairchild, to assist in this litigation. I was asked by Townsend to review the following U.S. Patents: 5,767,567 ("the '567 patent"), 5,907,776 ("the '776 patent"), and 5,930,630 ("the '630 patent"). Collectively, I refer to these patents as the AOS Patents. I was asked to provide expert opinion testimony that would assist the Court in determining the meaning of the claim terms of the AOS Patents.

Methodology

6. The first step in the course of my analysis was to read the AOS Patents. I then reviewed their file histories, including the cited prior art. At times, I also reviewed the extrinsic evidence cited by the parties, including relevant sections of dictionaries and technical books from the 1996 time frame for the '567 patent, and from the 1997 time frame for the '776 patent and '630 patent, as well as both earlier and later, to confirm the ordinary meaning of some of the terms.

7. I also reviewed the Joint Claim Construction And Pre-Hearing Statement ("the Joint Statement") that was filed on February 8, 2008. In Exhibit B of the Joint Statement, both parties present their proposed definitions for the claim terms, as well as the intrinsic and extrinsic evidence that the parties rely on in support of their respective definitions. Additionally, I reviewed AOS's Opening Claim Construction Brief, the Dr. Salama's declaration in support of AOS's opening brief, and the evidence cited AOS's supporting brief in support of AOS's proposed constructions. I also used this document to consider and analyze the proposed claim constructions of the parties.

Claim Meaning

8. In determining the meaning of the claims, I relied principally on the patents themselves, their file histories, the prior art cited in the patents, and the ordinary meaning of the claim terms at the time of the effective filing date of the patent applications. My analysis was done from the perspective of a person of ordinary skill in the art of the patents at the time of the filing of the applications for the AOS Patents, which is shown on the face of the patents as September 1996 for the '567 patent and July 1997 for the '776 patent and '630 patent.

9. I have reviewed Exhibit B of the Joint Statement, which sets forth the terms for which the parties have not agreed on a construction. I have analyzed each party's interpretation and support for the meanings of these disputed terms. I disagree with the proposed claim constructions offered in that document by Plaintiffs and Counterdefendants Alpha & Omega Semiconductor, Ltd., and Alpha & Omega Semiconductor, Inc. (collectively, "AOS"). Based upon my analysis and my understanding of how the term or limitation would be interpreted by a person of ordinary skill in the art at the time of the invention, I have determined that the claim constructions set forth by Fairchild are the correct interpretations.

Field Of The AOS Patents

10. The field of the AOS Patents, like the field of the Fairchild Patents, is power semiconductor devices such as power MOSFETs. I have provided a thorough summary of the general technology in my declaration in support of Fairchild's opening claim construction brief in this case. I respectfully refer the Court to my previous declaration for a discussion of the field of the patents.

'567 Patent

11. The '567 patent discloses methods for designing a power MOSFET device that is intended to allow for improved electrical contact between the device and the package in which it is encapsulated. A semiconductor device, such as a power MOSFET, is packaged in a protective structure after fabrication. The package serves two important purposes. First, it protects the device from damage. Second, it provides means to electrically connect the device to external circuitry, such as a printed circuit board.

12. Figure 1A of the '567 patent shows a top down view of an example of a semiconductor device packaged in a conventional package. While Figure 1A purports to be representative of the prior art, I am not familiar with any prior art products which resemble what is shown in Figure 1A. Nonetheless, I refer to this figure because it shows the basic structure of a chip package.

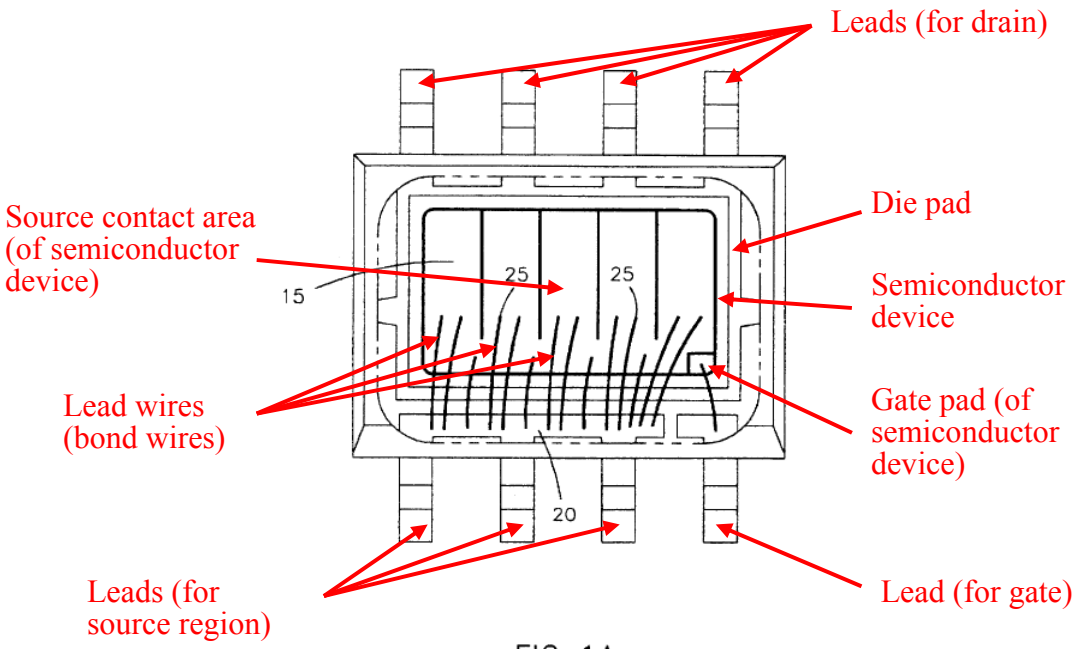


FIG. 1A
(PRIOR ART)

The semiconductor device is mounted on a metal structure called a leadframe, labeled 20 in Figure 1A. The leadframe includes a die pad and a number of leads, which are physically separate from the die pad. The semiconductor device is mounted directly on the die pad. In the case of a vertical power MOSFET (as is shown in all of the drawings of the '567 patent), in which the source regions and the gate are located near the top of the device, and in which the drain is located near the bottom of the device, a source contact area and a gate pad are located on the top surface of the device, and a drain is located on the bottom surface of the device. The source contact area and the gate pad are electrically connected to the leads by lead wires, labeled 25 in Figure 1A. In the device shown in Figure 1A, the source contact area is connected to the three leads on the bottom left and bottom center of the figure, and the gate is connected to the lead in the bottom right of the figure. The drain is electrically connected to the die pad on which it is mounted. The leads extend outside the package to facilitate electrical connection of the source region and the gate to outside circuitry, such as that on a printed circuit board. A number of leads connected to the die pad may also extend outside of the package to facilitate electrical connection of the drain to outside circuitry. In the device shown in Figure 1A, the source and gate leads extend out of the package at the bottom of the figure, and the drain leads extend

out of package at the top of the figure.

13. A vertical MOSFET often includes gate runners that are arranged on the source contact area. The gate runners distribute the gate voltage to the gate of the transistor. The gate runners are shown extending partially across the surface of the packaged device in Figure 1A of the ‘567 patent.

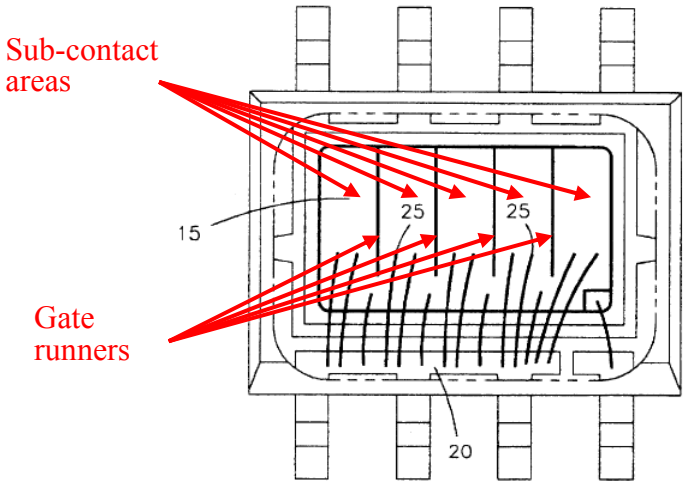


FIG. 1A
(PRIOR ART)

In the '567 Patent, the gate runners are described as dividing the source contact area into a number of sub-contact areas. In Figure 1A, four gate runners are shown extending partially across the source contact area, dividing it into five sub-contact areas. The arrangement of the gate runners, the relative areas of the sub-contact areas, and the distribution of lead wires within the sub-contact areas are important aspects of claim 7 of the '567 patent.

14. The method disclosed in the patent seeks to achieve a more uniform distribution of lead wires across the source contact area than in the prior art structure of Figure 1A. The desired goal of this distribution method is to improve the on-resistance of the device. On-resistance can be affected by many factors, including the thickness of the semiconductor substrate, the doping concentrations for the regions in the device, and the distance between adjacent cells. The ‘567 patent addresses a component of on-resistance that may be due to the arrangement of the source bonding wires on the top surface of the die. The patent teaches that the lead wires of Figure 1A are not evenly distributed throughout the source contact area, and this increases the on-resistance of the Figure 1A device. To

address the uneven distribution of lead wires on the source-contact areas, the patent teaches a technique for ensuring that the number of lead wires in each of the sub-contact areas is proportional to the relative size of each of the sub-contact areas. Thus, for example, larger sub-contact areas should have more lead wires distributed in them, and smaller sub-contact areas should have less lead wires distributed in them.

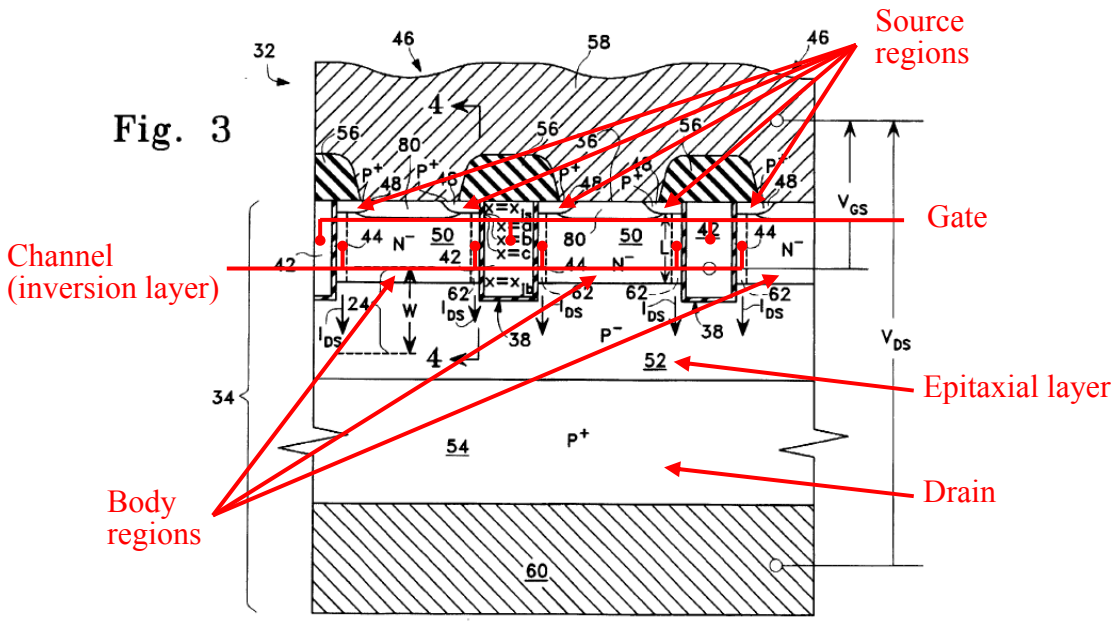
15. The '567 patent asserts that a problem with the prior art methods of designing power MOSFETs was that the design process did not take into account the packaging process. Thus, according to the patent, the prior art methods resulted in non-ideal distributions of lead wires in the source contact area. The method of arranging gate runners taught in the '567 patent takes the packaging process into account by first determining the total number of lead wires that will be used, and then arranging the gate runners to provide an even distribution.

16. The method taught in the '567 patent first determines the total number of lead wires that the device needs, which is limited by the maximum number of lead wires the leads can accommodate. The method then uses a mathematical formula, disclosed in column 4 of the patent, to determine the total number of lead wires that will be distributed in the each of the sub-contact areas. This formula takes into account the total number of gate runners the device needs to satisfy performance requirements. The method finally uses the ratios of lead wires distributed in the sub-contact areas as a guide for configuring the gate runners. Specifically, the ratios of the relative areas of the sub-contact areas must equal the ratios of the relative numbers of lead wires in the sub-contact areas. For example, the device described with respect to the preferred embodiment in Figure 2B of the patent includes four sub-contact areas, and the distribution of lead wires in the sub-contact areas is 4:4:4:3. Therefore, the gate runners are arranged on the source contact area so that the sub-contact areas have area ratios of 4:4:4:3.

'776 Patent

17. The '776 patent discloses a method for fabricating a power MOSFET that seeks to reduce the threshold voltage of the device by using a "compensating implant" into the body regions of the transistor. A cross-sectional illustration of a power MOSFET manufactured according to the disclosed invention is shown in Figure 3 of the patent:

Fig. 3



As can be seen in Figure 3, the device includes a number of source regions, a number of body regions, a drain, and a gate. (There appears to be more than one gate, but in fact the gate often is a single large interconnected structure of conductive material.) The source and drain regions are of the same conductivity type (P), but the body is of an opposite conductivity type (N). When the device is turned off, current cannot flow across the boundaries of opposite conductivity type. When the device is turned on, however, a channel region forms at the surface of the body region adjacent to the gate which has the same conductivity type as the source regions and the drain region, allowing current to flow between the source and drain regions.

18. The various regions in a semiconductor device, such as the one shown in Figure 3, are formed by a process called “doping.” The doping process usually involves bombarding the substrate with "impurity" or "dopant" ions at a particular energy and dosage in a process called ion implantation. Impurities may be implanted into the semiconductor substrate through a protective layer or mask. In that case, the impurities will be implanted only into those portions of the substrate that are not covered by the mask. Some important variables of importance in the implantation process are (1) the energy of the implant; (2) the dosage of the implant; and (3) the type of dopant being implanted; and (4) the type of material into which the dopant is being implanted. The energy of the implant

corresponds to the velocity of the ions to be implanted, and it affects the depth the ions penetrate into the substrate. Generally, the higher the energy, the deeper the impurities will travel into the substrate. The dosage, or quantity of implanted dopant ions, determines the effect of the implant on the material into which the impurities are implanted. For example, a high-dosage implant of one impurity type into a region that has an opposite conductivity type can convert the conductivity at the location of the implant from one conductivity type to the other. The same implant performed at a lower dosage, on the other hand, may be insufficient to change the conductivity type of the material at the location of the implant. Such a low-dosage implant may, however, change the properties of the material at the location of the implant. Specifically, the material may become less conductive than it was before. For example, a P+ region that is implanted with an N-type dopant at a low dosage may become a P- (P "minus", i.e. less "P") region, rather than converting to an N region.

19. The patent uses a "compensating" implant to reduce the threshold voltage of the device. The threshold voltage is minimum voltage that, when applied to the gate of the transistor, causes the transistor to turn on. When a voltage equal to or greater than the threshold voltage is applied to the gate, an inversion layer is formed in the portion of the body region that is adjacent to the gate. This inversion layer is the channel region shown above in Figure 3. When the channel is present, electrical current can flow through the channel between the source and the drain. When the voltage ceases to be applied to the gate, the channel region disappears and the device stops conducting electrical current.

20. Designers of power semiconductor devices, such as power MOSFETs, seek to obtain an optimal threshold voltage for the device. If the threshold voltage is too high, then the device will require more power to operate, since the voltage required on the gate to turn the device on is higher. On the other hand, if the threshold voltage is too low, then the device may turn on inadvertently, due to phenomena such as electrical noise in the gate. Thus, designers typically adjust several design parameters to achieve the desired threshold voltage. The '776 patent lists several of these parameters, specifically the gate oxide thickness, the impurity concentration in the body region, and the length of the channel region. This last variable, the length of the channel region, can be controlled by adjusting the depth of the body region and/or the depth of the source region.

21. The method disclosed in the '776 patent describes adjusting the threshold voltage of a power MOSFET by implanting impurities into the body region that are of the same conductivity type as the source region. This compensating implant – which is different from the implant used to form the source region – is performed at an energy level that is sufficiently high to cause the peak concentration of the implanted dopant ions to be found in the body region. Furthermore, according to the patent, the implant is at a dosage that is sufficiently low that it does not convert the conductivity type of the body region at the location of the compensating implant. Rather, it reduces the "net concentration" of dopants at the location of the implant in the body region. Thus, the compensating implant is different from the implant that formed the source region, which was at a sufficiently high dosage so as to convert the conductivity type at the location of the implant from one type to the other. Consequently, as described in the patent, the effect of the compensating implant is not to move the location junction between the source and the body region, which would shorten the channel region. Rather, the patent teaches making the portion of the body region near the source/body junction less conductive, thereby reducing the threshold voltage while leaving the length of the channel region unchanged.

'630 Patent

22. The '630 patent relates to a method of making power MOSFET devices. As I explained in detail in my declaration dated March 13, 2008, a power MOSFET device includes one or more gates. When the device is turned on by applying a voltage to the gate, current flows between the source and drain of the device through the channel that is formed adjacent to the gate. Power MOSFET devices typically have source regions, body regions, an epitaxial layer in which the source and body regions are formed, gate electrodes, and a substrate on which the epitaxial layer is deposited. The '630 patent relates to a method of making power MOSFET devices having purportedly enhanced ruggedness due to the presence of, among other things, a double implant step to form a "self-aligned shallow high concentration body dopant region" and a "self-aligned deep high concentration body dopant region." A representative embodiment from the specification is set forth below:

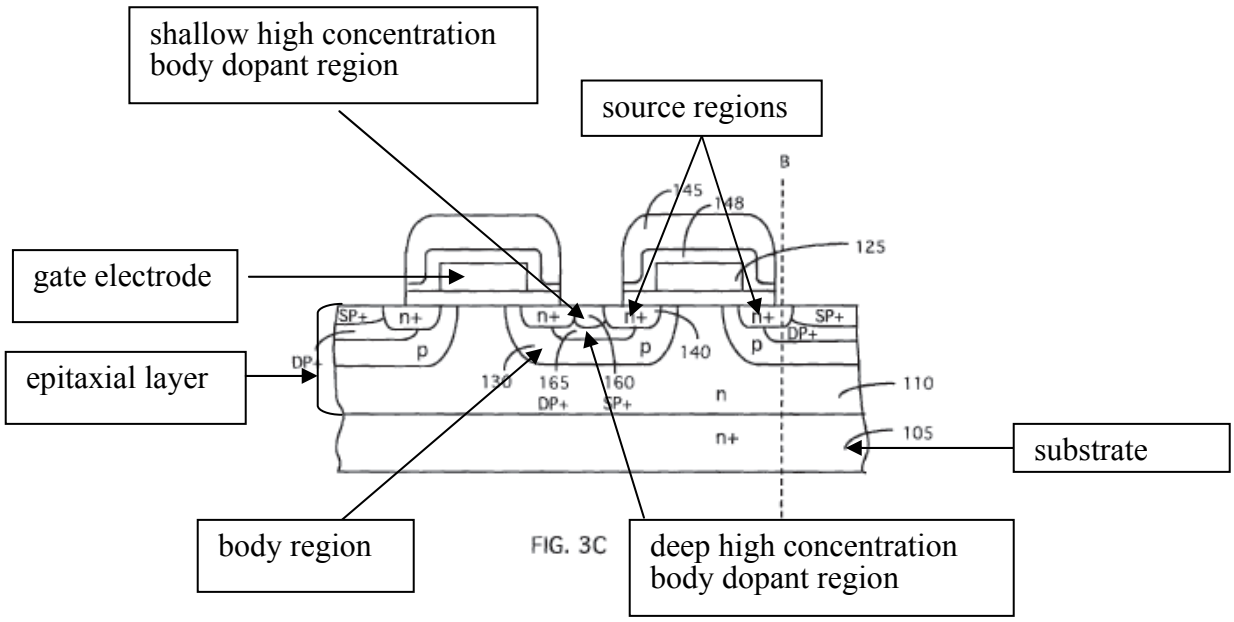


FIG. 3C

23. As shown in this annotated drawing, Figure 3C of the '630 patent discloses a power MOSFET including a substrate, an epitaxial layer formed on top of the substrate, and source and body regions formed in the epitaxial layer. It also includes gate electrodes formed on the surface of the epitaxial layer, as well as shallow and deep high concentration body dopant regions formed in the body region. This embodiment is referred to as a "planar" power MOSFET because the gates are formed on the top surface of the device instead of in trenches etched into an underlying material, as in the case of trench power MOSFETs.

Level Of Ordinary Skill In The Art Of The AOS Patents

24. In my opinion, the AOS Patents were addressed to a person with at least a bachelor's degree in electrical engineering or solid-state physics and having approximately three to five years of experience in the field of power semiconductor device design, or alternatively at least a master's degree in electrical engineering or solid-state physics and one to three years of experience in the same field. This person would readily understand the design of power semiconductor devices having trenched gates, and the formation of termination structures, as well as the affects that variations in the design of such structures have on the performance characteristics of the device. The person of ordinary skill would have the requisite knowledge that I described in the "Field Of The AOS Patents"

section above. The level of ordinary skill in the art for the AOS Patents is the same as that for the Fairchild Patents, as set forth in my prior declaration.

DISPUTED TERMS

CONFIGURING SAID GATE RUNNERS FOR DIVIDING SAID SOURCE CONTACT AREA INTO SEVERAL SUB-CONTACT AREAS WITH A SET OF AREA PROPORTIONAL RATIOS

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios	'567 patent, claim 7	arranging the gate runners, after determining the total number of lead wires, to define several sub-contact areas that are not all equal in size and such that the ratio of lead wires to area is the same for each of the sub-contact areas	the placement of gate runners divides the source contact area into sub-contact areas, and a set of area proportional ratios are defined by the ratios of the approximate areas of the sub-contact areas

25. Fairchild's proposed construction of the "configuring …" limitation is consistent with the understanding of a person of ordinary skill in the art in view of the '567 patent claims and specification. The term "configuring" as applied to arranging gate runners in a source contact area does not have any unique technical meaning to a person of ordinary skill in the art. The patent specification makes clear that the total number of lead wires must be determined before the gate runners are configured on the source contact area. Furthermore, a person of ordinary skill in the art would understand that the specification and file history limit the invention to arranging the gate runners such that the sub-contact areas are not all of equal size.

26. The background section of the '567 patent specification states in column 1, lines 25-37, that a problem with prior art techniques for power MOSFET design was that they did not take into account the how the device would subsequently be packaged. The patent points out that when the device is packaged, lead wires are attached to the device for making electrical connection between the transistor and the pins of the package (i.e., the "leads" described above). The patent also points out that the lead wires affect the performance characteristics of the of the packaged device, namely the on-resistance. Then, the patent states that because the power MOSFET is designed and packaged in two

separate steps, the affects of the packaging process on the performance characteristics of the device are not taken into account in the design process.

27. The patent teaches a method of designing a semiconductor device such as a power MOSFET that takes into account how the device will be packaged. In particular, the source contact area of the power MOSFET is designed so as to allow the lead wires to be evenly distributed. Specifically, the patent teaches a method in which the number of lead wires and the number of gate runners are determined before the gate runners are laid out, i.e., the number of lead wires and the number of gate runners must be determined before the gate runners are arranged on the source contact area. According to the patent, the total number of lead wires requires consideration of two factors: the number of lead wires the device needs, and the maximum number of lead wires the leads can accommodate. A person of ordinary skill in the art would understand that "the number of wires the device needs" depends upon the desired on-resistance of the device and the amount of current the device must supply. For example, if a particular device requires high current flow, then more lead wires are needed. The patent states that the total number of gate runners depends upon the "device characteristics." Specifically, for large devices, more gate runners are needed to evenly distribute the gate voltage to the gate structure, thereby reducing gate resistance and improving switching speed.

28. The patent teaches that the gate runners divide the source contact area into "sub-contact" areas. Accordingly, the total number of sub-contact areas is said to equal the total number of gate runners plus one. Although not mentioned in the patent, this assumes that the gate runners will be laid out in a generally parallel relationship. The patent discloses a formula by which the distribution of lead wires into the sub-contact areas is then computed. The formula simply requires dividing the total number of lead wires by the total number of sub-contact areas. This division generates two numbers -- a quotient and a remainder. The quotient, referred to in the patent as the "integer potion," is the minimum number of wires that will be present in each sub-contact area. The remainder is the number of sub-contact areas that will have one more lead wire than the minimum number of lead wires. As an example, if there are 19 lead wires and 5 sub-contact areas, 19 divided by 5 produces a quotient of 3 with a remainder of 4 (i.e. (3 x 5) + 4 = 19). Therefore, all of the sub-contact areas will have a minimum of 3 lead wires, and four of the sub-contact areas will have an additional lead wire.

So, one sub-contact area will have 3 lead wires, and four sub-contact areas will have 4 lead wires. This produces a lead wire distribution of 4:4:4:4:3. Finally, the gate runners are then distributed in the source contact area such that the relative sizes of the resulting sub-contact areas equal this distribution ratio (e.g., the relative areas of the sub-contact areas in the above example would be 4:4:4:4:3).

29. The method described in the patent for configuring the gate runners in the source contact area will work only if the total number of lead wires is determined ***before*** the gate runners are arranged. Without first knowing the total number of lead wires, the distribution ratio of lead wires into sub-contact areas cannot be determined. And without knowing the distribution of lead-wires into the sub-contact areas, there is no guidance as to how to arrange the gate runners so that the sub-contact areas have the desired sizes. I believe it is important to realize that the patent does not teach a random and arbitrary configuration of gate runners on the source contact area. Rather, the patent teaches a method of arranging gate runners so as to take into account the package that the device will be placed in after it is manufactured. Placement of gate runners before knowing the number of lead wires, and therefore not taking into account the total number of lead wires, is contrary to the purpose of this invention.

30. Furthermore, a person or ordinary skill in the art would understand the '567 patent to cover only arranging the gate runners such that at least one sub-contact areas is of a different size than the others. This is true in every embodiment described in the patent. In other words, the sub-contact areas that result from arranging the gate runners cannot all be the same size. The patent states at column 3, line 67 to column 4, line 5, that "[a]ccording a principle of this invention, in order to reduce the spread resistance, the topology of the gate runner 140 [is] specially arranged according to the location of the lead frames and the external pins, e.g., pin 1 to pin 4, for dividing the source contact areas 150-1 to 150-4 to source contact areas ***of unequal sizes***." (Emphasis added). The formula described in column 4 teaches how to arrange the sub-contact areas so as to have unequal sizes. No formula is needed to create sub-contact areas having equal sizes. In fact, it was well known in the art prior to the filing of the '567 patent to use sub-contact areas of equal size (as is shown in Figure 1A), and to distribute the source current as evenly as possible. I believe that AOS's proposed construction, which would cover sub-contact areas having equal sizes, would cover this prior art.

COMPENSATING A PORTION OF SAID BODY REGION BY IMPLANTING MATERIAL OF SAID SECOND CONDUCTIVITY TYPE IN SAID BODY REGION

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
compensating a portion of said body region by implanting material of said second conductivity type in said body region	'776 patent, claims 1, 13, and 25	implanting impurities of the second conductivity type into the body region such that the peak concentration of that implant is located in the body region, and such that the conductivity type at the location of the peak concentration of that implant does not change	implanting into the body region material having conductivity type opposite the conductivity type of the body region

31. Fairchild's proposed construction of the "compensating" limitation is consistent with the understanding of a person of ordinary skill in the art. In particular, Fairchild's proposed construction reflects the understanding of a person of ordinary skill in the art that the location of an implant is considered to be the location of the peak concentration of the implant. Fairchild's proposed construction also requires that the implant not convert the conductivity type of the body region at the location of the implant's peak concentration (i.e., change P to N or vice versa). AOS's proposed construction, on the other hand, is overly broad and covers prior art techniques that have nothing to do with the invention disclosed in the '776 patent. AOS's construction would cover an implant that moves the location of the source/body boundary. The patent, however, teaches away from this.

32. The claims of the '776 patent require that a compensating dopant material be implanted at a particular location, i.e., "in said body region." In accordance with the understanding of a person of ordinary skill in the art, Fairchild's proposed construction recognizes that a dopant implant is "located" where its peak concentration occurs. When impurities are implanted into a semiconductor device, the impurities do not all penetrate into the material the exact same distance. Rather, the impurities are spread out in a distribution that closely approximates a Gaussian curve having a familiar bell-shaped distribution with a "peak" at the center of the distribution curve. This is shown, for example, in FIG. 5 of the '776 patent, which shows three such implant curves 70A, 70B and 70C. The peak of the curve is the location of the highest concentration of the implanted dopants, and the position of this peak is understood by those skilled in the art to be the location of the implant. The

dopant concentration diminishes with increasing distance from the central peak. Because the edges of a Gaussian curve tail off slowly, a small but measurable number of dopant atoms are implanted a distance from the peak. The location of the peak and the shape of the dopant distribution curve depend primarily on the energy of the implant, the type of dopant being implanted, and the type of material into which the dopant is being implanted. As one would expect, a higher implant energy causes the peak concentration of the implant to be located deeper into the substrate, whereas a lower energy causes the peak to be located closer to the surface. A person of ordinary skill in the art would consider the location of the implant to be where the peak concentration occurs, not the entire broad range of locations over which any dopant ion might exist after the implantation. It is important to define the location of the compensating body region implant to distinguish it from the implant that is used to create the adjacent source region. The claim language itself states that the compensating implant is made "in said body region" and "proximal to said source region." (Claim 1, col. 9, lns. 14-17). As I explain below, the peak of the compensating implant must be located outside of the source region so that its depth is beyond the depth of the source/body junction. In a source implant the peak is, obviously, located in the source, but because implanted ions are distributed in a near-Gaussian distribution, a relatively low concentration of atoms far from the peak will end up in the body region.

33. The terms used by persons of ordinary skill in the art to describe an implant are: (1) projected range, and (2) standard deviation. Contrary to what intuition might suggest, the "projected range" is not a range at all, but rather is a single value. Specifically, it is the location of the peak concentration of the implant. The standard deviation (σ), as in all Gaussian distributions, is a measure of the percentage of dopants that are located within a particular distance of the peak concentration. For example, a high percentage of the implanted dopants is located between 0 and 1σ, a lower percentage is located between 1σ and 2σ, an even lower percentage is located between 2σ and 3σ, etc.. A person of ordinary skill in the art would understand that the location of an implant is considered to be its projected range, i.e. the location of the peak concentration of the implant. Fairchild's proposed construction takes this understanding into account.

34. This understanding of the location of an implant is supported by the '776 patent specification itself. The '776 patent specification repeatedly refers to the "penetration distance" or the

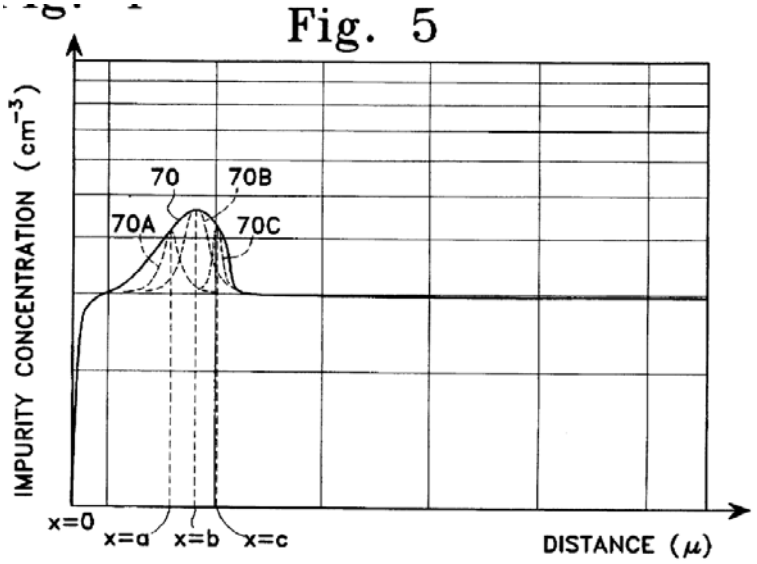
"distances from the planar surface" of each of the individual implants that form the compensating implant as being at a specific depth, namely x=a, x=b, and x=c. For example, column 5, lines 50-61 the patent state that:

> Shown in FIG. 5 is the resultant impurity concentration profile represented by a compensation curve 70 which in essence is a superimposition of three individual implantation curves 70A-70C. The ***penetration distances*** of the individual implantation x=a, x=b, and x=c are first determined. The process of ion implantation is employed to place various dosages of dopant into the substrate 34. An exemplary technique for implanting a dopant at a ***predetermined penetration distance*** into a silicon substrate can be found in a publication by Wolf et al., "Silicon Processing for the VLSI Era", Lattice Press, IEEE Transactions on Electron Devices, Vol. 1, pages 285-291.

(Emphasis added). Similarly, column 7, lines 39 to 56 of the patent state that the three implants that form "compensation curve 70" are located at a specific distance from the planar surface, and specify that the distances are x=a, x=b, and x=c:

> The step of body region compensation is the next step in the fabrication process. Reference is now directed back to FIGS. 3-5. To secure a reasonably level body diffusion curve 66 near the body junction $x=x_{js}$, ***successive implantations at various distances from the planar surface*** 36 (FIG. 3) are preferred. It this method, boron ions are ***implanted at distances of x=a, x=b and x=c from the planar surface*** 36 (FIG. 3), which distances correspond to the individual implant profiles 70A, 70B and 70C, respectively, as shown in FIG. 5. Profile 70B can be higher in amplitude and can be coincident with the peak value of the body diffusion curve 66 had the curve 66 not been compensated (that is, the uncompensated curve 30). Once the ***distances x=a, x=b and x=c*** are determined, the corresponding implant energy levels can be extracted from the energy chart as shown in FIG. 6. Boron is then driven into the structure as shown in FIG. 7J by the process of ion-implantation in which implant dosages are set by the implant durations.

Figure 5 of the patent shows that the values x=a, x=b, and x=c correspond the location of the peak concentration of each implant.



It is important to note that the '776 patent never refers to any of the three implants identified as 70A, 70B and 70C in Figure 5 as "compensating implants." Rather, it merely refers to them as "individual implant profiles." According to the patent specification, Figure 5 shows "the resultant impurity concentration profile represented by a compensation curve 70 which in essence is a superimposition [sic] of three individual implantation curves 70A-70C." The patent repeatedly refers to curve 70 as the "compensation curve." For this reason, one does not look at any of the individual implants shown in Figure 5 as providing the location where "compensation" occurs. Instead, one must look at the location of the aggregate of the individual implants.

35. Furthermore, the chart shown in Figure 6 and the corresponding text in the patent also make clear that the location of the implant is where its peak concentration occurs. This chart shows the energy that must be used to achieve a particular implant depth by providing the depth of the peak concentration of an implant (for varying dopant types) at different energy levels. The patent states at column 5, line 62 to column 6, line 6 that:

> FIG. 6 shows a graphical representation of the relationship between the ***penetration distance*** and the ***required energy implantation energy level***. For example, in this embodiment, boron (B) is used as the implant material. As an illustration, suppose a ***distance of 0.3 μ of penetration distance beyond the planar surface*** 36 (FIG. 3) is intended. Once the ***desired penetration distance 0.3 μ is located*** at the ordinate axis of FIG. 6, the corresponding value on the abscissa axis can be extracted. As shown in FIG. 6, the ***required energy level*** for the implanting boron is 83 KeV. In a similar manner, positioning implant materials at other ***penetration distances*** can likewise be determined.

Again, the penetration distance of a species at a particular implant energy is given as a single value, not as a range. Thus, the patent describes the location of the implants that, in the aggregate, form the compensating implant as being located where the peak concentration of the implant occurs.

36. Furthermore, Figures 4 and 5 and the corresponding text in the specification of the '776 patent make clear that the peak of the compensating implant in the preferred embodiment is located in the body region. The patent states at column 7, lines that:

> The step of body region compensation is the next step in the fabrication process. Reference is now directed back to FIGS. 3-5. To secure a reasonably level body diffusion curve 66 near the body junction $x=x_{js}$, successive implantations at various distances from the planar surface 36 (FIG. 3) are preferred. It this method, boron ions are implanted at distances of x=a, x=b and x=c from the planar surface 36 (FIG. 3), which distances correspond to the individual implant profiles 70A, 70B and 70C, respectively, as shown in FIG. 5. ***Profile 70B*** can be higher in amplitude and can be ***coincident with the peak value of the body diffusion curve 66 had the curve 66 not been compensated (that is, the uncompensated curve 30)***.

Figure 4 shows that the peak value of the uncompensated curve 30 (shown as a dashed line) is located to the right of the source-body junction, identified as $x=x_{js}$ in Figure 4. Figure 5 shows that the peak value of profile 70B is at the same location as the peak value of the compensation curve 70.

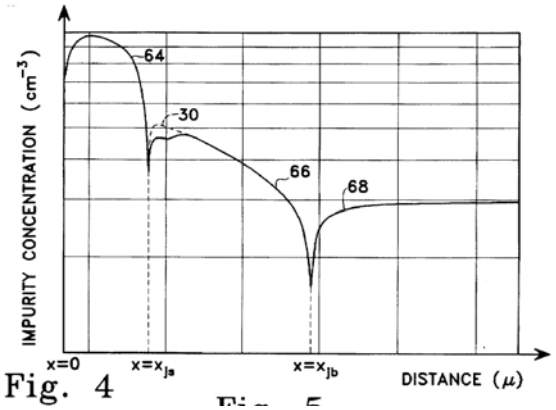


Fig. 4

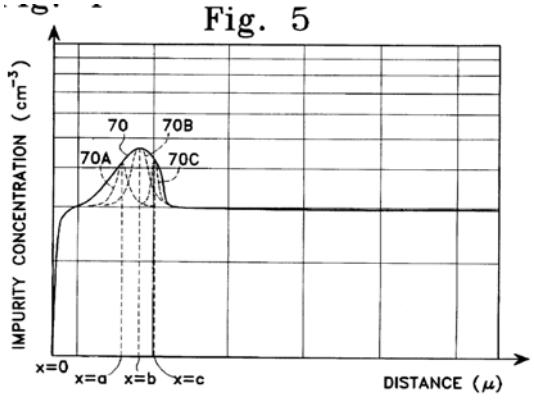


Fig. 5

Since the peak value of implant profile 70B (and therefore also the peak profile of compensation curve 70) in Figure 5 is at the same location as the peak location of uncompensated curve 30 in Figure 4, it necessarily follows that the peak value of the compensation curve 70 is located in the body region, not in the source region. This is consistent with the claim language which states that the compensating implant is made "in said body region."

37. AOS's proposed construction does not provide a specific location of the compensating implant. Therefore, it covers any implant in which some dopant ends up in the body region, no matter how few dopant atoms actually end up in the body region, and no matter where the peak dopant concentration is located. Thus, an implant having a peak concentration in the source region, that results in only a few dopant atoms reaching the body region, would fall within AOS's proposed construction. A person of ordinary skill in the art would not interpret the '776 patent claims as covering an implant in which the peak dopant compensation is located in the source region. Such an implant would not create a compensated region in the body region. Rather, it would simply increase the depth and/or impurity concentration of the source region. Therefore, performing an implant having a peak concentration in the source region (as opposed to in the body) would have the same effect as diffusing the source region deeper into the device – they would both push the source-body junction deeper into the device, shortening the length of the channel region. The patent, at column 3 lines 23 to 31 and, specifically teaches away from diffusing the source region deeper into the device because the resulting decrease in channel length (shown in Figure 2) can cause problems with punch-through. Since an implant having a peak concentration in the source region would lead to the same problems identified with regard to prior art techniques involving longer source diffusions, a person of ordinary skill in the art would read the patent specification as teaching away from AOS's proposed construction.

38. Fairchild's proposed construction also requires that the compensating implant not convert the conductivity type of the body region at the location of the peak concentration of the implant. This is consistent with the understanding of a person of ordinary skill in the art. A compensating implant causes the net concentration of impurities in the compensated region to decrease. An implant that converts the conductivity type would not create a "compensated" region, but rather would simply result in a deeper source region. A person of ordinary skill in the art would not consider an implant that deepens the source region to be a "compensating" implant.

39. I have reviewed the extrinsic evidence cited by AOS in support of its proposed construction of the "compensating" limitation. None of this extrinsic evidence supports AOS's proposed construction. The IEEE dictionary defines "doping compensation" as "[a]ddition of donor

impurities to a p-type semiconductor or of acceptor impurities to an n-type semiconductor." This definition says nothing about converting the conductivity of the semiconductor from one type to another, and therefore cannot be read as supporting AOS's proposed construction. The Wiley Electrical and Electronics Engineering Dictionary (2004) defines "compensated semiconductor" as "[a] semiconductor with two types of impurities or imperfections, in which the electrical effects of one type of impurity or imperfections ***partially cancel*** the other. For instance, a donor impurity ***partly annulling*** the electrical effects of an acceptor impurity." (Emphasis added). The language "partially cancel" and "partially annul" actually refutes AOS's proposed construction and support Fairchild's. If the compensating implant could convert the conductivity of the semiconductor from one type to another, the definition would say "completely cancel" or "completely annulling" or some similar language. Even the declaration of Dr. Salama supports Fairchild's proposed construction by stating that "[w]hen a semiconductor region is compensated, the introduced dopants ***partially cancel*** the pre-existing dopants of the opposite conductivity type." (Emphasis added). In my opinion, AOS has provided no evidence whatsoever in support of its assertion that a compensating implant can convert the conductivity type of the semiconductor material.

APPLYING A POLYSILICON MASK FOR ETCHING SAID POLYSILICON LAYER TO DEFINE A PLURALITY OF POLYSILICON GATES

Disputed Term	Patent and Claim(s)	Fairchild's Proposed Construction	AOS's Proposed Construction
applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates	'630 patent, claim 1	applying a mask having a plurality of openings to allow the removal of areas of a polysilicon layer to form a plurality of polysilicon gates corresponding to the plurality of areas of the mask which are not open	the meaning of this phrase is clear and unambiguous to a person of skill in the art, and thus it need not be construed by the court

40. I understand the parties dispute the meaning of the term "applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates" as used in claim 1 of the '630 patent. For the reasons set forth below, a person of ordinary skill in the art would understand the term to mean "applying a mask having a plurality of openings to allow the removal of areas of a polysilicon layer to form a plurality of polysilicon gates corresponding to the plurality of areas of the

mask which are not open."

41. The disputed language appears in paragraph (b) of claim 1 of the '630 patent. Claim 1 relates to a method for making a MOSFET on a substrate, and paragraph (b) of the claim states:

> applying an active mask for etching said active layer to define an active area followed by ***depositing an overlaying polysilicon layer*** thereon and ***applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates***

The key claim language is in bold. The claim requires, among other things, the step of depositing a polysilicon layer. Polysilicon is a conductive material from which the gates are formed. The claim further requires that, after the polysilicon layer is deposited, the gates are "defined" in the polysilicon layer by applying a polysilicon mask for etching the polysilicon layer.

42. Claim 1 refers to four separate masks used in the claimed process. The first mask (an "active mask") is used to define the active area. The active area is the area of the chip in which the active transistor cells are formed (as opposed to the periphery of the chip). The second mask (a "polysilicon mask") is used to define the polysilicon gates that become part of the active transistor cells. The third mask (a "source blocking mask") is used to define the locations of the source implants within each of the active transistor cells. The fourth mask (a "contact mask") is used to define the locations of the contact openings that are positioned between the gates in the active transistor cells.

43. The specification explains what it means to "define" polysilicon gates in the polysilicon layer through the use of a mask. It discloses that the process for making polysilicon gates begins with the formation of a structure which includes a semiconductor substrate, an epitaxial layer deposited on the substrate, and an initial oxide layer formed on a portion of the epitaxial layer ('630 patent, col. 6, line 67 - col. 7, line 9). The initial oxide layer covers the entire surface of the die, and then an "active mask" is used to open up the active area by exposing it to an etch. (*Id.*). The active area is shown to the left of the "initial oxide layer" shown as feature 115 below. If one were to look down on the die from above, the active area would look like a generally square area of exposed epitaxial layer surrounded by the initial oxide layer.

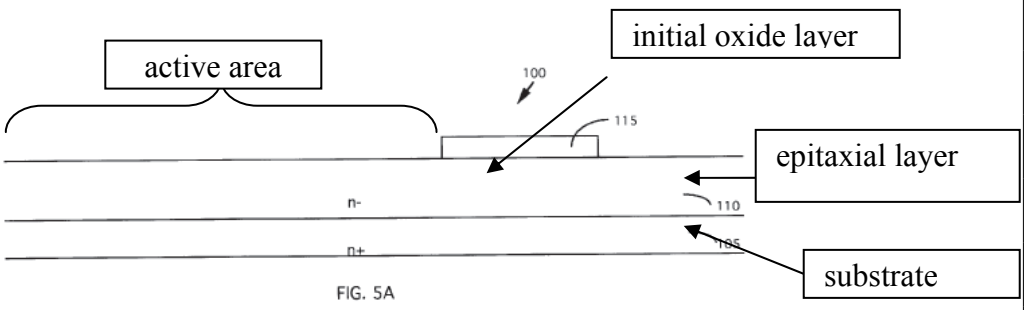


FIG. 5A

('630 patent, Fig. 5A (annotated)).

44. The specification further teaches that a gate oxide layer is then grown on the top surface of the substrate, and that a polysilicon layer is subsequently deposited on the gate oxide layer, thereby covering the top surface with polysilicon material ('630 patent, col. 7, lines 9-12):

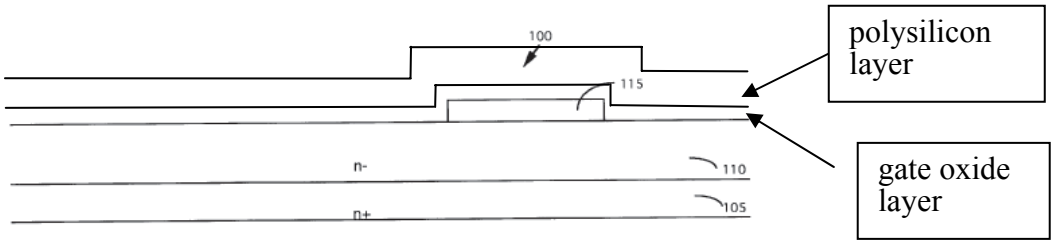


FIG. 5A

('630 patent, Fig. 5A (annotated)). I supplemented the above figure from the specification to illustrate the polysilicon layer and gate oxide layer described in the text of the specification.

45. The specification further discloses that, after the deposition of the polysilicon layer, a polysilicon mask is used to define the polysilicon gates, by etching (removing) portions of the polysilicon layer where the gates will not be present. ('630 patent, col. 7, lines 14-16 ("A polysilicon mask is then applied to carry out the an anisotropic etching process to define the polysilicon gate 125.")). This step, in turn, results in the presence of polysilicon gates on the top surface of the structure, and the shapes of the polysilicon gates correspond to the shapes of the areas of the mask which are not open:

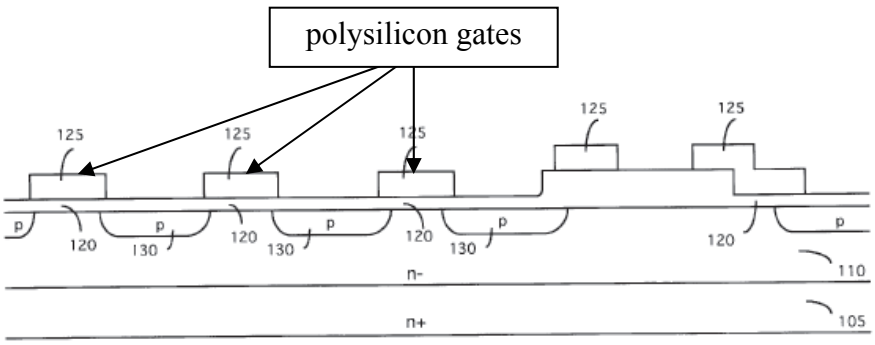


FIG. 5B

('630 patent, Fig. 5B (annotated)).

46. In view of the foregoing, a person of ordinary skill in the art would understand the term "applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates" to mean "applying a mask having a plurality of openings to allow the removal of areas of a polysilicon layer to form a plurality of polysilicon gates corresponding to the plurality of areas of the mask which are not open." Moreover, the specification does not disclose or suggest any other way in which polysilicon gates are "defined" in a polysilicon layer through the use of a mask for etching.

47. I disagree with AOS's interpretation of this term. AOS appears to contend that the claim term should be interpreted by breaking it into three phrases, and interpreting each phrase individually. AOS's position appears to be that the claim simply requires each of these steps to be performed (i.e., "applying a polysilicon mask," "etching" the polysilicon layer, and "defining" polysilicon gates). I therefore understand that AOS believes the claim covers a process in which a polysilicon mask is used, even if the features of the mask do not correspond to the shape of polysilicon gates which are formed. AOS's interpretation is incorrect. The claim language requires a relationship between the mask and the shape of the polysilicon gates. Indeed, the claim language combines these steps into a single phrase. ('630 patent, col. 9, lines 65-67 ("applying a polysilicon mask ***for*** etching said polysilicon layer ***to*** define a plurality of polysilicon gates")). The specification also confirms the claimed invention requires a relationship between the shape of the mask and the shape of the gates. As explained above, the specification discloses a process for making polysilicon gates where the shape of the gates correspond to the areas of the mask that are not open.

48. I disagree with AOS's interpretation for the additional reason that it is based on a

flawed interpretation of the requirement that the polysilicon mask be used "to define" the polysilicon gates. As explained above, the specification discloses that a polysilicon mask is used to define polysilicon gates when portions of the polysilicon layer are removed corresponding to the areas of the mask that are not open. In other words, the shapes of closed areas of the mask correspond to the shapes of the polysilicon gates. AOS, however, contends that the meaning of "define" depends on whether the gate is planar or trench. AOS asserts that a mask defines the gates of a planar MOSFET based on the horizontal dimension of the gates, whereas the mask defines the gates of a trench MOSFET based on the vertical dimension. I disagree.

49. A person of ordinary skill in the art would not understand the word "define" to have a different meaning for different structures. Instead, it has a specific meaning which is explained in the specification. As discussed above, a mask has areas which are open and ones that are not. The openings in the mask correspond to areas in the polysilicon layer that are etched. The mask, therefore, defines the polysilicon gates by permitting some areas of the polysilicon layer to be etched, which results in polysilicon gates corresponding to the areas of the mask which are not open.

50. I disagree with AOS's argument that a polysilicon mask can define a trenched gate by establishing the vertical dimension of the gate. AOS's argument is based on the false premise that a polysilicon mask may be used to define a vertical dimension of a trenched gate. For a trenched gate device, a polysilicon mask plays no role at all in defining the gate. Instead, the gate is defined by the shape of the trench formed in the underlying material prior to the deposition of the gate material, which is typically polysilicon.

51. The specification of U.S. Patent No. 6,429,481 ("the '481 patent"), for example, describes a typical process for making the gates in a trench power MOSFET device. The first step is the etching of trenches into an underlying epitaxial layer:

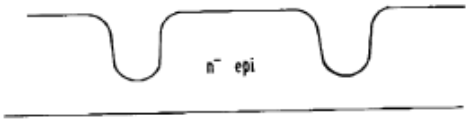


FIG. 4D.

The next step is the growth of a thin gate oxide layer and a polysilicon layer. The polysilicon layer fills the trenches and also covers the top surface of the device:

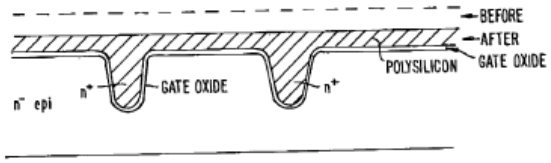


FIG. 4E.

The next step is the application of a mask to the device. The mask exposes the active area as a whole. Accordingly, the mask does not define the gates in the trenches. It is instead used to define other structures on the surface of the substrate, typically gate runners and pads which connect the MOSFET with the outside world. After the mask is applied, an etching process is performed to etch away portions of the polysilicon layer corresponding to the areas of the mask that are open. This results in most of the polysilicon layer on the surface of the substrate being etched away, while some polysilicon remains in the trenches:

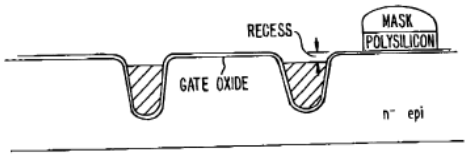
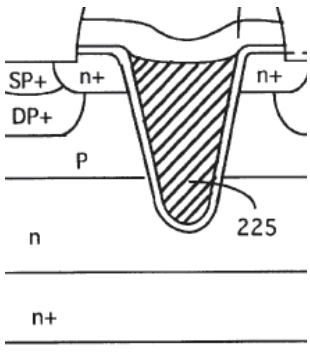


FIG. 4F.

As noted above, the polysilicon mask plays no role in establishing the shape of the gates. In fact, the gates would have the same structure even if no polysilicon mask were used. This is because the polysilicon mask is open across the trenches, which results in the entire polysilicon layer deposited in and around the trenches being exposed to the etching process, which is the same result that would take place if no polysilicon mask were used at all.

52. I disagree with AOS's description of the process used to make the gates in Figure 6 of the '630 patent. The relevant portion of Figure 6 is set forth below:



In describing this figure, AOS states:

> Prior to etching, there was polysilicon "gate" material that extended further vertically. A mask covered other regions of the substrate, so that it only exposed the gate. Etching removed the excess gate material from the substrate surface above the trench, thus defining the gate's vertical dimension. *See* '630 patent, Fig. 6.

(AOS Opening Brief, p. 16). This description is not correct. The

specification does not disclose a step of applying a mask that ***only*** exposes the gate. The specification does not describe at all how the gates illustrated in the figure are made. Nevertheless, a person of ordinary skill in the art would understand that the gates are not made as AOS suggests. As discussed above, trenched gates are typically formed by etching the epitaxial layer to form the trenches, forming a gate oxide layer and depositing a gate material (usually polysilicon) in the trenches and on the surface of the substrate, and then exposing the entire active area, including all the trenches, to an etching process. A polysilicon mask is not typically used to expose only the gate when making trenched gates. Moreover, if AOS's description were accurate, polysilicon material would be present on the surface of the substrate adjacent to the gate, as those areas would not be exposed to an etching process. No such layer is present. This further confirms that AOS's description of Figure 6 is inaccurate.

53. The vast majority of the specification relates to power MOSFET designs having a planar configuration. A very small fraction of the specification -- one figure and 20 lines of text -- describes a trench power MOSFET design. ('630 patent, Fig. 6 & col. 8, line 55 - col. 9, line 7). The description of the trench device relates to the use of shallow and deep self-aligned high concentration body implants, which is the focus of the claimed invention. The specification does not describe how to form gates in the trench device.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct to the best of my knowledge and belief. Executed this 27th day of March, 2008, in Mountain View, California.

Richard A. Blanchard

Richard A. Blanchard, Ph. D.

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